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Patent Office
Notice of Reason for Rejection

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Application No.: 10-2001-0012568

Title of the Invention: Semiconductor Device and Method of Manufacturing It

Since the following reason(s) for rejection has been found according to the examination of this application, this notice are made under patent law section 63. If necessary, please file a written opinion and/or amendment by the due date indicated above. (You may request every one-month extension of time period, however, no notice of accepting the extension of time regarding this request will be made.)

[Reason(s)]

The invention(s) recited in claims 1-3 and 7-10 of this application could easily have been made, prior to the filing of the patent application, by a person with ordinary skill in the art to which the invention pertains. Therefore, the invention(s) shall not be granted for a patent under patent law section 29(2).

Claims 1-3 and 7-10 relates to a semiconductor device comprising a gate electrode on a semiconductor layer of a first conductive type, high concentration source/drain regions of a second conductive type adjacent to the gate electrode, and a drift region of the second conductive type surrounding the drain region, and characterized in that an impurity layer of the second conductive type is formed to be adjacent to the drain region.

This could easily have been made by a person having ordinary skill, by utilizing the structure of a high voltage MOS bipolar transistor having three deferent p-type drain regions disclosed in the cited publication 1, U.S. Patent No. 5,229,308, and the structure of a high voltage MOSFET including a graded junction at the drain region from high concentration to low concentration disclosed in the cited publication 2, U.S. Patent No. 4,290,077.

[Enclosure]

Enclosure 1 U.S. Patent No. 05229308 (July 20, 1993)

Enclosure 2 U.S. Patent No. 04290077 (September 15, 1981)

September 6, 2002

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